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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,157	10/20/2000	Jang-Ho Cho	SAM-162	8192

7590 11/15/2004

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/693,157	CHO, JANG-HO	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2004 and 13 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been examined.

Response to Amendment

2. The drawing objections have all been overcome by the filed amendment filed 9/13/04 and are thus withdrawn.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/03/04 has been entered.

Claim Objections

4. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. A table, or specifically an accuracy history table in this case, inherently is made up of a memory array and thus by stating that the table of claim 1 includes a memory array, claim 4 is not further limiting.

5. Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper

dependent form, or rewrite the claim(s) in independent form. Claim 8 states, "...the predicted accuracy signal is determined by a most significant bit of the at least one accuracy history bit," while claim 1 states, "...the predicted accuracy history signal being a most significant bit of the at least one accuracy history bit...". The independent parent claim in this case actually has a more narrow a scope since it defines the accuracy history signal to be the same as a most significant bit and claim 8 says that the signal is determined by the most significant bit. Thus since claim 8 is broader than the parent claim, it cannot further limit it.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Manne (Branch Prediction using Selective Branch Inversion).

8. In regard to claim 1, Manne discloses a branch predictor comprising:

a. Branch prediction means for predicting a conditional branch instruction (figure 6);

b. A comparator for generating a comparison signal by comparing the predicted conditional branch from the branch prediction means with a real conditional branch of the branch instruction; [The Examiner is taking the term "real condition branch" to be the actual outcome of the branch instruction and

whether it was take or not taken. Refer to section 2.2, paragraph 1, lines 16-18 where Manne discloses a branch being correctly predicted. A comparator would have been inherently used to determine if the branch was correctly predicted by comparing the prediction with the actual outcome.]

c. An accuracy history table for storing an accuracy history of the predicted conditional branch; [Manne also discloses an accuracy history table (confidence estimator table of Figure 6) for storing an accuracy history of the predicted conditional branch. Section 1, paragraph 1 shows that confidence estimation assesses the quality of a prediction, in other words, its accuracy.]

d. A first state transition logic circuit for generating at least one accuracy history bit to be stored to the accuracy history table in response to the comparison signal; [Section 2.2 shows that accuracy history tables or confidence estimators are updated based on counters. Figures 3 and 4 show that a confidence or accuracy signal is simply high or low and thus a single bit]

e. And a multiplexer for outputting an alternative one of the conditional branch prediction and an inverted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on the at least one accuracy history bit, the predicted accuracy history signal being a most significant bit of the at least one accuracy history bit and being directly applied to a selection control input of the multiplexer to select between the conditional branch prediction and the inverted conditional branch prediction. [Figure 6 shows a select and invert box that receives the branch prediction and confidence

estimator values as inputs. The included dictionary definition of "multiplexer" in a digital environment (definition 3) states that a multiplexer is a device selects and outputs one of a number of inputs. Figure 6 includes the logic equation for the select and invert function. This function when illustrated as a circuit would be an OR gate receiving inputs from two AND gates, where the first AND gate receives the branch prediction "b" as well as the second confidence estimation "c1", and the second AND gate receives the inverted branch prediction and the inverted first confidence estimation"c0". The inverted values are inverted by a pair of inverters to form the "invert" portion of the "select & invert" function. The select portion or multiplexer is the remaining circuitry, which based on the dictionary definition given above, selects the branch prediction or its inverse based on selection by confidence estimation. As shown in figures 3 and 4, the confidence estimation or accuracy history signal are composed of a single bit and thus this signal is the most significant and only significant bit. As shown in the above argument, the accuracy history signal or bit "c1" from the corresponding table of figure 6 is directly applied to the multiplexer to select a branch prediction or its inverse.]

9. In regard to claim 2, Manne discloses the branch predictor according to claim 1, wherein the branch prediction means comprises:

a. A branch history register for storing conditional branches of previous instructions; [Manne shows in section 2.1 and 4.2 that the Gshare predictor of Figure 2a is used as the branch predictor portion of Figure 6 in one embodiment.

Manne discloses the use of a branch history register in the Gshare predictor for storing the outcome of previous branch instructions as described in section 2.1, paragraph 2.]

b. A pattern history table for storing pattern history bits used for generating the predicted conditional branch corresponding to the conditional branches of the previous branch instructions stored in the branch history register; [Figure 2a shows the use of a pattern history table that corresponds to previous conditional branch outcomes with the Gshare predictor that produces a branch prediction.]

c. And a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction. [The two-bit counter scheme, a standard in the Gshare predictor, of section 2.1, paragraph 2 serves as a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction.]

10. In regard to claim 3, Manne discloses the branch predictor according to claim 2, wherein the second state transition logic circuit includes an up/down saturating counter. [This counter is by nature up/down counting so the pattern history can change based on both a taken and not-taken branch. The counter in this algorithm is also inherently of the saturating type so that a counter of the strong taken state ('11') does not roll over to the strong not-taken state ('00') because of another taken branch, but instead stays at the strong taken state.]

11. In regard to claim 4, Manne discloses the branch predictor according to claim 1, wherein the accuracy history table includes a memory array. [This is inherent as described above in the objection.]

12. In regard to claim 5, Manne discloses the branch predictor according to claim 1, wherein the comparator generates the comparison signal having a first logic value when the predicted conditional branch is the same as the real conditional branch, and generates the comparison signal having a second logic value when the predicted conditional branch is different from the real conditional branch. [The saturating counter of the above argument requires a different value to be received from the inherent comparator discussed above for a correct prediction than an incorrect prediction. A '1' will increase the count by one and a '0' decrease it, or visa versa. If a different value is not given for correct or incorrect, the counter will eventually be stuck at either the upper or lower extremities with no way to count in the other direction.]

13. In regard to claim 6, Manne discloses the branch predictor according to claim 1, wherein the first state transition logic circuit includes an up/down saturating counter. [Manne keeps a count of correct predictions in his accuracy history table using a first state logic circuit that includes a saturated up/down counter (paragraph 4 of section 4.1, the up/down counter is saturated because it is not a resetting counter, which is also described in this section).]

14. In regard to claim 7, Manne discloses the branch predictor according to claim 6, wherein the first state transition logic circuit is used after learning the predicted branch accuracy of patterns of previous branch instructions. [The first state logic counter

described above will be used after learning the accuracy of past pattern predictions since the comparator output (prediction outcome) is the activating signal and it determines if the past predictions were correct or not.]

15. In regard to claim 8, Manne discloses the branch predictor according to claim 1, wherein the predicted accuracy signal is determined by a most significant bit of the at least one accuracy history bit (as shown above).

Response to Arguments

16. Applicant's arguments filed 13 September 2004 have been fully considered but they are not persuasive.

17. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

18. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in the previous Office Action remains pertinent and is cited herein with this Action as well as the following pertinent reference.

US Pat No 6,092,187 to Killian teaches prediction selection based on confidence or accuracy metrics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
November 10, 2004

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